What is claimed is:

1. A method for forming a top metalization system for high performance integrated circuits, comprising:

forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of first metal lines in one or more layers;

depositing a passivation layer over said interconnecting metalization structure;

depositing an insulating, separating layer over said passivation layer that is substantially thicker than said passivation layer;

forming openings through said insulating, separating layer and said passivation layer to expose upper metal portions of said overlaying interconnecting metalization structure;

depositing metal contacts in said openings; and

forming said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of top metal lines, in one or more layers, each of said top metal lines having a width substantially greater than said first metal lines.

2. The method of claim 1 wherein the top metalization system connects portions of said interconnecting metalization structure to other portions of said interconnecting metalization structure.

3. The method of claim 1 wherein said top metalization system comprises signal lines that are substantially wider than lines in said interconnecting metalization structure.

4. The method of claim 1 wherein said top metalization system comprises power planes having power buses that are substantially wider than lines in said interconnecting metalization structure.

5. The method of claim 1 wherein said top metalization system comprises ground planes having ground buses that are substantially wider than lines in said interconnecting metalization structure.

6. The method of claim 1 wherein said top metalization system comprises planes that contain both signal lines and power buses that are substantially wider than lines in said interconnecting metalization structure.

7. The method of claim 1 wherein said top metalization system comprises planes that contain both signal lines and ground buses that are substantially wider than lines in said interconnecting metalization structure.

8. The method of claim 1 wherein said top metalization system comprises planes that contain both power buses and ground buses that are substantially wider than lines in said interconnecting metalization structure.

9. The method of claim 1 wherein said overlaying interconnecting metalization structure comprises electrical contact points.

10. The method of claim 9 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um.

11. The method of claim 1 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

12. The method of claim 1 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

13. The method of claim 1 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0